REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-8 are pending in the present application. Claims 1, 3, and 5 are independent claims.

Objection to the Specification

The objection to the minor informalities on pages 15, 16, and 26 respectively, has been corrected. Specifically, the occurrences of the phrase, "low-sensitivity digital signal Hb" has been corrected to read, ---low-sensitivity digital signal La--- on pages 15 and 16, and --- low-sensitivity digital signal Lb--- on page 26, respectively. The specific changes are shown in the attached replacement sheets.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, 3, 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over ***Kutner*** (US Patent No. 4,786,968) in view of ***Masaya*** (Japanese Patent No. 2001-008104). Applicant respectfully traverses this rejection.

In regards to claims 1 and 3, the Examiner relied on the CPU 10 in ***Kutner*** (Col. 2, lines 57-64) as the table overwriter to overwrites an LUT written into the table storage area (RAM) with another LUT. Applicant respectfully submits that ***Kutner*** does not disclose the "overwriting step/table overwriter" as claimed in claims 1 and 3 respectively. Specifically, the CPU 10 in ***Kutner*** merely downloads and stores the calculated gamma corrected lookup values x into the lookup table memory circuit RAM based on the input digital variable "a" input into CPU 10. The

Kutner device does not overwrite the LUT already stored in the table storage area with another LUT as specifically claimed. In contrast, the present invention has the feature of, *inter alia*, storing one of the LUTs for correcting gray-scale correction of a high-sensitivity digital signal, correcting gray-scale correction of a low-sensitivity digital signal, and a weighing LUT for signal synthesis, one at a time. This particular feature has the advantage of decreasing the memory area and chip size of the table storage area, thereby reducing the overall costs. The ***Masaya*** reference does not remedy this deficiency. ***Masaya*** was cited merely to show the synthesizing of a first digital signal and a second digital signal. Thus, for at least the reason mentioned above, Applicant believes claims 1 and 3 as originally claimed are patentably distinguishable over the ***Kutner*** and ***Masaya*** references. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

In regards to claims 5 and 6, ***Masaya*** does not disclose the plurality of first photoreceptor devices and second photoreceptor devices respectively each having a first photoreceptive area and a second photoreceptive area having different sensitivities as is now claimed. As shown in Fig. 2 of the present application, each of the photoreceptor devices 22 has a first photoreceptive area and a second photoreceptive area (m,s) having different sensitivities. The ***Masaya*** device shown in Fig. 2 merely discloses a plurality of photoreceptors (H, L) having different sensitivities. Further, ***Kutner*** fails to disclose the table overwriter as claimed in claim 5 for at least the reason as mentioned above in regards to claims 1 and 3. Accordingly, for the above reasons, Applicant believes claims 5 and 6 are patentably distinguishable over the ***Kutner*** and ***Masaya*** references. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 2, 4, 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over ***Kutner*** (US Patent No. 4,786,968) in view of ***Masaya*** (Japanese Patent No. 2001-008104), and further in view of ***Utagawa*** (US Patent No. 6,529,640). Applicant respectfully traverses this rejection.

Claims 2, 4, 7 and 8 are dependent from independent claims 1, 3 and 5 respectively. Applicant respectfully submits that ***Utagawa*** does not remedy the deficiencies of the table overwriter and the plurality of first photoreceptor devices and second photoreceptor devices respectively each having a first photoreceptive area and a second photoreceptive area having different sensitivities as claimed in independent claims 1, 3 and 5 respectively. Thus, Applicant submits that claims 2, 4, 7 and 8 are allowable at least by virtue of their dependency on claims 1, 3 and 5. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Conclusion

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but to merely show the state of the art, no comment need be made with respect thereto.

In view of the above amendment, applicant believes the pending application is in condition for allowance. Thus, the Examiner is respectfully requested to reconsider the outstanding rejections and issue a Notice of Allowance in the present application.

However, should the Examiner believe that any outstanding matters remain in the present application, the Examiner is requested to contact Applicants' representative, D. Richard

Anderson (Reg. No. 40,439) at the telephone number of the undersigned in order to discuss the application and expedite prosecution.

Dated: **August 16, 2007**

Respectfully submitted,

By _____

D. Richard Anderson
Registration No.: 40,439
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Rd
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

Attachments: Annotated sheets showing changes to the Specification

ANNOTATED SHEETS SHOWING CHANGES

On page 15, starting from the 1st line, please replace the first paragraph with the following paragraph:

---in the direction of column. The vertical transfer sections 24 are provided laterally on both sides of each column of photoreceptor devices 22. The vertical transfer section 24 separately reads the signal charge of the main region m and the signal charge of the sub-region s in the direction of column and transfers the signal charges to the horizontal transfer section 26. The horizontal transfer section 26 receives signal charges transferred from a plurality of vertical transfer sections 24 and transfers the received signal charges in the direction of row. The output section 400 outputs a voltage signal corresponding to the amount of the signal charge transferred from the vertical transfer section 26. Hereinafter, a plurality of voltage signals generated based on a plurality of charge signals from a plurality of main regions m are called a high-sensitivity signal H. A plurality of voltage signals generated based on a plurality of charge signals from a plurality of sub-regions s are called a low-sensitivity signal ~~H~~ L. The high-sensitivity signal H and the low-sensitivity signal L are sent to the A/D imaging processor 30.---

On page 16, starting from the 1st line, please replace the first paragraph with the following paragraph:

--- signals in 12-bit gray scale, and a high-sensitivity digital signal Ha and a low-sensitivity digital signal ~~Hb~~ La are generated respectively. The high-sensitivity digital signal Ha and the low-sensitivity digital signal ~~Hb~~ La thus generated are sent to the signal processor 50.---

On page 16, please replace the third paragraph with the following paragraph:

--- The signal processor 50 performs optimization of the high-sensitivity digital signal Ha and a low-sensitivity digital signal ~~Hb~~ La and synthesizes the high-sensitivity digital signal Ha and a low-sensitivity digital signal ~~Hb~~ La thus optimized to generate image data. The signal processor 50 is connected to the bus 110. The image data generated is recorded onto a recording medium 105 connected to the image recording/playback section 100 via the compressor 60 or bus 110. The signal processor 50 will be detailed later.---

On page 26, please replace the third paragraph with the following paragraph:

---Multipliers 260, 270 are circuits for multiplying a high-sensitivity digital signal Hb and a low-sensitivity digital signal Lb obtained after gray-scale conversion by the weighting factors h_gain and l_gain, respectively. The high-sensitivity digital signal Hb and the low-sensitivity digital signal ~~Hb~~ Lb which have undergone multiplication in the multipliers 260, 270 are summed up in an adder 280 to generate a synthesis signal S. The synthesis signal S output from the adder 280 is checked for an overflow by a limiter 290, then output as a final synthesis signal S from the optimum synthesis circuit 52 to the YC processor circuit 56.---